Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A signal processing circuit intended to be stacked with two mixer circuits, said signal processing circuit being intended to receive a pair of input signals in phase opposition on two input terminals and to provide two pairs of output currents in phase opposition on four output terminals intended to be connected to said two mixer circuits in order that each mixer circuit receives one pair of output currents in phase opposition, each input signal being amplified by a respective low noise amplification unit and being split by a respective splitting unit, characterized in that each of the two splitting units includes two branches connected between the respective amplification unit and one of the four output terminals, the four branches each including at least an impedance having identical characteristics.

2. (currently amended) A signal processing circuit as claimed in Claim 1, wherein each of the four branches of the two splitting units are further configured to exhibit an impedance, wherein the impedance has a resistance value such that said value determines the splitting of the input signal independently of the stacked mixer circuits.

3. (previously presented) A signal processing circuit as claimed in claim 1, wherein each of the four branches further includes a cascode transistor, bases of said four cascode transistors being connected together.

4. (previously presented) A signal processing circuit as claimed in claim 1, wherein each of the two amplification units includes at least one amplification transistor, of which the base is connected to one input terminal and the collector is connected to a respective splitting unit.

5. (previously presented) A signal processing circuit as claimed in claim 1, wherein each of the two amplification units includes at least an amplification transistor, of which the base is connected to one input terminal and the collector is connected to another transistor in cascode, said transistor in cascode being connected by its collector to a respective splitting unit and being connected by its base to the transistor in cascode of the other amplification unit.

6. (previously presented) A chip intended to be implemented in a receiver, said chip including at least a signal processing circuit and two mixer circuits receiving local oscillation signals in phase quadrature, said output terminals of said signal processing circuit being connected to said mixer circuits in such a way that each mixer circuit receives a pair of signals that are in phase opposition, characterized in that said signal processing circuit is as claimed in claim 1.

7. (original) A receiver of radio-frequency signals including at least an antenna, a reception chain, a processing unit, characterized in that it includes a chip as claimed in claim 6.

8. (new) A signal processing circuit intended to be stacked with two mixer circuits, said signal processing circuit being intended to receive a pair of input signals in phase opposition on two input terminals and to provide two pairs of output currents in phase opposition on four output terminals intended to be connected to said two mixer circuits in order that each mixer circuit receives one pair of output currents in phase opposition, each input signal being amplified by a respective low noise amplification unit and being split by a respective splitting unit, characterized in that each of the two splitting units includes two branches connected between the respective amplification unit and one of the four output terminals, the four branches each including at least an impedance having identical characteristics, wherein each of the two amplification units includes at least an amplification transistor, of which the base is connected to one input terminal and the collector is connected to another transistor in cascode, said transistor in cascode being

connected by its collector to a respective splitting unit and being connected by its base to the transistor in cascode of the other amplification unit.

9. (new) A signal processing circuit as claimed in Claim 8, wherein each of the four branches of the two splitting units are further configured to exhibit an impedance, wherein the impedance has a resistance value such that said value determines the splitting of the input signal independently of the stacked mixer circuits.

10. (new) A signal processing circuit as claimed in claim 8, wherein each of the four branches further includes a cascode transistor, bases of said four cascode transistors being connected together.

11. (new) A chip intended to be implemented in a receiver, said chip including at least a signal processing circuit and two mixer circuits receiving local oscillation signals in phase quadrature, said output terminals of said signal processing circuit being connected to said mixer circuits in such a way that each mixer circuit receives a pair of signals that are in phase opposition, characterized in that said signal processing circuit is as claimed in claim 8.

12. (new) A receiver of radio-frequency signals including at least an antenna, a reception chain, a processing unit, characterized in that it includes a chip as claimed in claim 11.